	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	176	(ohmic adj contact) same Ni same Ti	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 15:56
2	BRS	L2	7	(ohmic adj contact) and (InGaAs same Ni same Ti)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 15:56

	Type	Hits	Search Text	DBs	Time Stamp
1	BRS	1251	(ohmic adj contact) and (InGaAs or InAs or InGaP)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/12 14:17
2	BRS	611	((ohmic adj contact) and (InGaAs or InAs or InGaP)) and (Ti or Mo or W or TiW or silicide or borides)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 09:41
3	BRS	1678	(ohmic adj contact) and (InGaAs or InAs or InGaP or InP or InAlAs or InGaASP or GaSb or InGaSb) and (Pt or Pd or Ru or V or Au or Co or Ti or Mo or W or TiW or silicide or borides)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 09:41
4	BRS	144	((ohmic adj contact) and (InGaAs or InAs or InGaP or InP or InAlAs or InGaASP or GaSb or InGaSb) and (Pt or Pd or Ru or V or Au or Co or Ti or Mo or W or TiW or silicide or borides)) and HBT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 09:42

	Type	Hits	Search Text	DBs	Time Stamp
5	BRS	50	(((ohmic adj contact) and (InGaAs or InAs or InGaP or InP or InAlAs or InGaASP or GaSb or InGaSb) and (Pt or Pd or Ru or V or Au or Co or Ti or Mo or W or TiW or silicide or borides)) and HBT) not (((ohmic adj contact) and (InGaAs or InAs or InGaP or InP or InAlAs or InGaASP or GaSb or InGaSb) and (Pt or Pd or Ru or V or Au or Co or Ti or Mo or W or TiW or silicide or borides)) and (heterojunction adj bipolar adj transistor))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 09:43
6	BRS	131	((ohmic adj contact) and (InGaAs or InAs or InGaP or InP or InAlAs or InGaASP or GaSb or InGaSb) and (Pt or Pd or Ru or V or Au or Co or Ti or Mo or W or TiW or silicide or borides)) and (heterojunction adj bipolar adj transistor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/09/13 09:43

DOCUMENT-IDENTIFIER: US 6235547 B1
TITLE: Semiconductor device and method of fabricating the same

BSPR:
For instance, there can be found many reports wherein the quantum wire
structure is fabricated by forming a stripe mask on a (001) face of a III-V
group compound semiconductor such as GaAs and InP, either etching exposed
areas, which are not covered by the stripe mask, to thus form a so-called
V-shaped groove section and then growing a multilayered semiconductor film
constituting the hetero junction structure or growing the multilayered
semiconductor film directly on the (001) face of the III-V group compound
semiconductor in areas, which are not covered by the stripe mask.

BSPR:
FIGS. 41A and 41B show a natural forming technique of the quantum dot. An
AlGaAs buffer layer 212 and a GaAs layer 213 are formed in that order by
epitaxial growth on a GaAs substrate 211 having (111) surfaces. An InGaAs
layer 214 in which In composition is set to about 0.5 so as to have large
lattice mismatching is grown on the GaAS layer 213, and a GaAs layer 215 is
grown thereon. By either selecting growth temperature or executing annealing
process after the epitaxial growth, spherical areas 216 having large In
composition are generated in the InGaAs layer 214. The spherical areas 216 are
generated naturally, and have

Appl. Phys.
Lett. 65 (1994), pp.1421-1423

BSPR:
In addition, Marzin et al. have reported that the quantum dot can be derived by
growing the **InAs** layer and the GaAs layer on the (100) GaAs substrate by means
of MBE.[7]J. Y. Marzin et al., Phys. Rev. Lett. 73 (1994), pp.716-719

BSPR:
[8] H. **V.** Schreiber et al.: Electron Letters, vol.25, 1989, p.185

BSPR:
More specifically, concave sections, having an inverse regular tetrahedron
shape or its similar shape, is first formed by means of the photolithography
etc. on a (111)B face or (111)A face substrate of a III**-V** group semiconductor
or on a substrate having face orientation similar to the III**-V** group
semiconductor. The III**-V** group semiconductor has a zincblend type crystal
structure. Then, selective growth or regrowth of a semiconductor in respective
concave sections is effected by a growth method like MBE, MOVPE or ALE (Atomic
Layer Epitaxy), thus resulting in the quantum structure. Note that the inverse
regular tetrahedron (triangular pyramid) can be formed by utilizing an
extremely small etching rate in a [1 1 1]A face or a (111)B face in contrast to
those in other faces.

DEPR:
As a material constituting the substrate, III**-V** group compound semiconductor
may be used, for example. As

DEPR:
Further, as a III-V group compound semiconductor film formed by epitaxial
growth, either a ternary mixed crystal such as AlGaAs, **InGaAs, InAlAs, InGaP,**
AlGaAs or AlGaP or a quaternary mixed crystal such as AlGaAsP, InGaAlAs,
InGaAlP, or **InGaAsP** as well as the binary system compound such as GaAs, **InP,** or
GaP may be used. Note that a multilayer-stacked structure may be used as the
compound semiconductor film.

DEPR:
As a material of the semiconductor layer, a II-VI group compound semiconductor
such as zinc-selenide (ZnSe), zinc-telluride (ZnTe), and cadmium-telluride
(CdTe) may be used in addition to the III-V group semiconductor layer.

DEPR:
An A-face of a group III-V compound semiconductor is the group III element, and
a B-face of the group III-V compound semiconductpor is the group V element.

DEPR:
Next, a detailed method of forming concave sections in the (111)B face of the
GaAs (III-V group semiconductor) substrate will be explained as a definite
example.

DEPR:
In the meanwhile, according to the experiment by the present inventors, the
concave sections 9a to 9c formed by the etching solution employing the mask on
the GaAs substrate 6 are not always formed as the regular

apex on the bottom resides along the [1 1 1] A face thereof. On the other
hand, in the concave sections (not shown) of regular tetrahedron formed on the
InP substrate in the same manner, three triangular faces in the **InP** substrate
become almost plane faces, so that cubic shapes which are very close to the
regular tetrahedrons could be always derived. In this case, the Br.sub.2
--C.sub.2 H.sub.5 OH having a volume concentration of 1% has been used as the
etching solution for the **InP** substrate.

DEPR:
Now, there may be an insulating film such as SiN, SION, or a conductive film
such as **W,** WSi in addition to the SiO.sub.2 film as a mask material. Note that
any mask material having good close contact to the compound semiconductor layer
and causing no undercut in the substrate may be used. Further, the
semiconductor material, which can be obtained by stacking different kind of
semiconductors and employing a certain enchant that enables selective etching,
may be used as a mask. For instance, there are **InGaP** formed on the GaAs,
InGaAs formed on the **InP** and the like.

DEPR:
In the above described explanation, the growth rate of the arsenic containing
compound semiconductor layer has been varied on the [1 00] face, the (111)B
face and [1 1 1] A face by changing the arsenic supply amount. Note that such
characteristic is not limited to the arsenic containing compound semiconductor.
In case the compound semicondu

ments

In case the resonance tunneling diode having the quantum box structure is formed by the photolithography technology, reduction of power consumption and operation at room temperature are raised as problems. In order to reduce the power consumption, a ratio (P/V ratio) of peak value (P value) to valley value (**V** value) in a substantially N-shaped differential load curve, which appears in a current (I)-voltage (**V**), must be increased. In this case, since the valley current specifies consumption current while storing information, it is necessary to reduce the **V** value. In addition, in order to realize the operation at room temperature, a large difference between the P value and the **V** value is needed. However, the resonance tunneling diode structure formed by the photolithography technology is formed as a plan rectangular shape having one side of almost 1 .mu.m, which is large in contrast to de Broglie wavelength (almost 10 nm) of electron. Therefore, since, in the lateral direction, the diode structure is not formed as a quantum size, it has been difficult in principle to improve the P/V ratio.

DEPR:
In the second embodiment, the P/V ratio can be set larger then the conventional one by forming the double barrier structure in the quantum box formed in the bottom of the concave section. More specifically, by forming the double barrier structure as the quantum box which is the zero-dimensional quantum well, the valley value (**V** value) in the I-**V** characteristic appearing as an

of the resonance tunneling diode formed by the two-dimensional quantum well
structure, it can be so understood that, even under the non-resonance voltage
condition, the so-called valley current flows from the emitter to the collector
because a high energy state electron subband (extension of a wave function from
the emitter side) formed in the quantum well is shifted to a low energy state
electron subband (extension of a wave function from the collector side) owing
to emission of the LO phonons.

DEPR:
In turn, several definite examples of **InP** system quantum semiconductor memory
device will be explained.

DEPR:
Referring to FIGS. 15A to 15E and FIG. 16, steps of fabricating a first **InP**
system quantum semiconductor memory device will be discussed. FIGS. 15A to 15E
are sectional views taken along the bit line.

DEPR:
First, as shown in FIG. 15A, an n.sup.+ type **InGaAs** sub collector layer 48 of
200 nm in thickness, an n type **InGaAs** collector layer 49 of 200 nm in
thickness, an i type **InP** collector barrier layer 50 of 100 nm in thickness, an
n type **InGaAs** base layer 51 of 50 nm in thickness, and an Fe doped
semi-insulating **InP** layer 52 of 500 nm in thickness are continuously and
epitaxially grown on the (111) B face of an semi-insulating **InP** substrate 47
having the zincblende type crystal structure by means of reduced pressure MOVPE

the etching
mask previously, an **InAlAs** barrier layer 56 of a thickness of 3 nm, an **InGaAs**
well layer 57 of a thickness of 4 nm, and an **InAlAs** barrier layer 58 of a
thickness of 3 nm are grown in the concave section so as to trace the shape of
the concave section. Thereafter, an n type **InGaAs** emitter layer 59 and n.sup.+
type **InGaAs** contact layer 60 are grown so as to bury remaining section of the
concave section.

DEPR:
In this case, if such growth conditions (i.e., growth temperature and **V** group
element supply amount) are selected that the growth rate of the [1 1 1] A face
as the side face of the concave section is set extremely larger than that of
the (111)B face corresponding to the crystal face in the bottom face of the
concave section, these layers may be grown so as to trace the shape of the
concave section.

DEPR:
Note that n.sup.+ type **InGaAs** contact layer 60 may be formed by an ion
injection method.

DEPR:
Next, as shown in FIG. 15E, a double emitter structure having a first emitter
61 and a second emitter 62 are defined by etching process. A mesa structure 63
reaching an n.sup.+ type **InGaAs** sub-collector layer 58 is formed. Then, an
emitter electrode 64 connected to an n.sup.+ type **InGaAs** contact layer 60 in
the emitter side via a contact

DEPR:
An Fe-doped semi-insulating **InP** layer 52 grown on an n type **InGaAs** base layer
51 is processed by anisotropic etching using an SiO.sub.2 film 53 as the mask
to thus form a concave section having an inverse regular triangular
tetrahedron. After this, an i type **InP** barrier layer 66, an i type **InGaAs** well
layer 57, and an i type **InP** barrier layer 67 are grown in the concave section
so as to trace the shape of the concave section. Thereafter, an n type **InGaAs**
emitter layer 59 and an n.sup.+ type **InGaAs** contact layer 60 are grown so as to
bury remaining section of the concave section.

DEPR:
In other words, in the second embodiment, the i type **InAlAs** barrier layer 56,
58 in the first embodiment are replaced with the i type **InP** layers 66, 67.
Therefore, since carriers can be confined by high-resistance of the
semi-insulating **InP** layer 52 constituting the concave section, such
replacements are enabled while keeping the same device characteristic as in the
first embodiment.

DEPR:
In this case, note that the n.sup.+ type **InGaAs** contact layer 60 may also be
formed by the ion injection method.

DEPR:
A p type or i type **InP** layer 68 is grown on an n type **InGaAs** base layer 51.
Thereafter, the p type or i type InP layer is processed by

concave section. Thereafter, an n type **InGaAs** emitter layer 59 and an n.sup.+
type **InGaAs** contact layer 60 are grown so as to bury remaining section of the
concave section.

DEPR:
More particularly, in this third embodiment, the semi-insulating **InP** layer 52
in the first embodiment is replaced with the p type or i type **InP** layer 68.
Therefore, since carriers can be confined by high diffusion barrier or
high-resistance of the p type or i type **InP** layer 68, such replacement is
enabled while keeping the same device characteristic as in the first
embodiment.

DEPR:
In this case, note that the n.sup.+ type **InGaAs** contact layer 60 may also be
formed by the ion injection method.

DEPR:
A p type or i type **InGaAs** layer 69 is grown on an n.sup.+ type **InGaAs** base
layer 51. The p type or i type **InGaAs** layer 69 is processed by anisotropic
etching using an SiO.sub.2 film 53 as the mask to thus form a concave section
having an inverse regular triangular tetrahedron. After this, an i type **InAlAs**
or InP barrier layer 70, an i type **InGaAs** well layer 57, and an i type **InAlAs**
or InP barrier layer 71 are grown in the concave section so as to trace the
shape of the concave section. Thereafter, an n type **InGaAs** emitter layer 59
and an n.sup.+ type **InGaAs** con to

with the i type
InAlAs or InP barrier layers 70, 71. Therefore, since carriers can be confined
by high diffused barrier and high-resistance of the p type or i type **InGaAs**
layer 69, such replacements are enabled while keeping the same device
characteristic as in the first embodiment.

DEPR:
An n.sup.+ type **InGaAs or InP** layer 72 is grown on an n type **InGaAs** base layer
51. The n type **InGaAs or InP** layer 72 is processed by anisotropic etching
using an SiO.sub.2 film 53 as the mask to thus form a concave section having an
inverse regular triangular tetrahedron. After this, an i type **InAlAs or InP**
barrier layer 70, an i type **InGaAs** well layer 57, and an i type **InAlAs or InP**
barrier layer 71 are grown in the concave section so as to trace the shape of
the concave section. Thereafter, an n type **InGaAs** emitter layer 59 and an
n.sup.+ type **InGaAs** contact layer 60 are grown so as to bury remaining section
of the concave section.

DEPR:
In particular, in the fifth embodiment, the semi-insulating **InP** layer 52 in the
first embodiment is replaced with the p type or i type **InGaAs** layer 69. In
addition, the i type **InAlAs** barrier layers 56, 58 are replaced with the i type
InAlAs or InP barrier layers 70, 71. Therefore, since the n type semiconductor
layer is used to form the concave section and, therefore, a diffused barrier
for electrons as carriers becomes sufficiently effect

positive-biased relatively, a lowest potential barrier can be derived locally
in the bottom section of the concave section. Thus, since the quantum box
which has an effective carrier confine dimension less than a dimensional limit
specified by its geometrical dimension can be achieved, electrons may be
injected into the base layer from this smallest section.

DEPR:
As shown in FIG. 21C, if the n type **InGaAs** base layer 51 of the semiconductor
device is biased relatively positively and the n type **InGaAs** emitter layer 59,
i.e., the n.sup.+ type **InGaAs** contact layer 60 is biased relatively negatively,
an electric field near the bottom of the concave section having a small radius
of curvature is emphasized. Thus, a potential for electrons in that section
becomes minimum as shown in FIG. 21C.

DEPR:
In this case, in order to form the concave section, a semiconductor layer, for
example, a semi-insulating **InP** layer of a thickness of 0.2 .mu.m is formed on
an n type **InGaAs** base layer. An SiO.sub.2 film 53 is then formed on the
semi-insulating **InP** layer. A plurality of regular triangular opening sections
54 (the number is 48 in FIG. 22) having a side of 0.3 .mu.m are in turn formed.
Next, like the first embodiment, the double barrier structures are formed by
etching and epitaxial growth processes in the concave sections 55.

DEPR:
If the n sup.+ type **InGaAs** lay

formed near the
bottom.

DEPR:
In the first example, a thickness of the semi-insulating **InP** layer 52 having
the concave sections therein is set as 0.5 .mu.m. However, the thickness is
not limited to this value, and may be set to any value within a range of 10 nm
to 10 .mu.m. Further, thicknesses of the barrier layers and the well layer
constituting the double barrier structure may be set to any value within a
range of 1 to 10 nm and a range of 1 to 50 nm, respectively. These ranges can
also be used in the second to fifth examples.

DEPR:
In the sixth example, a thickness of the semi-insulating **InP** layer 52 having
the concave sections therein is set as 0.2 .mu.m. However, the thickness is
not limited to this value, and may be set to any value within a range of 10 nm
to 10 .mu.m. In addition, thicknesses of the barrier layers and the well layer
constituting the double barrier structure may be set to any value within a
range of 1 to 10 nm and a range of 1 to 50 nm, respectively.

DEPR:
In the above first to sixth examples, a GaAs system semiconductor may be used
instead of the **InP** system material used. In other words, a semi-insulating
GaAs substrate may be used instead of the semi-insulating **InP** substrate, a GaAs
layer may be used instead of the **InGaAs** layer, an AlGaAs layer may be used
instead of the **InP** barrier lay

GaAs system, and can be applied in principle to a semiconductor having the zincblende type crystal structure. For instance, a binary compound semiconductor such as GaP, a ternary compound semiconductor such as AlGaAs, **InGaAs, InAlAs, InGaP,** AlGaP, a quaternary compound semiconductor such as **InGaAsP** may be employed. In addition, a II-VI group compound semiconductor having the zincblende type crystal structure may be utilized.

DEPR:
As shown in FIG. 23B, the GaAs substrate 151 is etched via an SiO.sub.2 mask 152 by anisotropic etching using ethanol solution including bromine of 1 volume (**V**) %. (111) A faces 155 of the GaAs substrate 151 are scarcely etched by the 1 **V** % Br.sub.2 -ethanol solution. Therefore, the GaAs faces exposed from the opening portions 153 of the mask 152 are gradually etched, but etching on the (111) A faces does not proceed any longer after the (111) A faces are exposed. If the etching is continued further, it ceases automatically at the time when triangular pyramid which is circumscribed about the opening portion 153 is formed, as shown in FIG. 23B. In this state, a cavity 154 having the triangular pyramid shape surrounded by side faces, which have three-fold rotational symmetry formed by the (111) A faces, is formed on the lower portion of the opening portion 153. In addition, three ridgelines meet together at the top portion 156 of the triangular pyramid. Face orientation at the meeting portion is not defined exactly, but changes gradually. Now, the top portion

vapor phase epitaxy (LP-MOVPE) at a growth atmospheric pressure of 50 torr.
When the epitaxial growth is executed, a V/III ratio of supply gas is set to
two values 191 and 19 upon growing the GaAs layer, and a V/III ratio of supply
gas is set to two values 170 and 17 upon growing the **InGaAs** layer. These
growth temperatures are set respectively to two values, i.e., 600.degree. C.
and 700.degree. C.

DEPR:
As shown in FIG. 24A, a GaAs buffer layer 157 having a thickness of about 30
nm, an **InGaAs** quantum well layer 158, and a GaAs cap layer 159 having a
thickness of about 20 nm have been grown on the inner surface of the concave 4
on the GaAs substrate 151 covered with the SiO.sub.2 mask 152 in that order. A
thickness of the **InGaAs** quantum well layer 158 has been varied between 2.5 to
50 nm. A density of the tetrahedral-shaped concaves (TSR) is about 1.times.106
cm.sup.-2.

DEPR:
FIG. 25A shows the result of the PL measurement. The abscissa shows photon
energy to emit light in unit of eV while the ordinate shows strength of PL
light in arbitrary unit. The PL strength is shown by a curve pl1 in FIG. 25A
in case a thickness of the **InGaAS** layer 8 on the (111) A faces is 50 nm. In
FIG. 25A, two peaks have been observed at energy 1.4 eV and energy 1.46 eV.
Energy difference 60 meV between two peaks cannot be verified by quantum size
effect. Based on the quantum be

prepared.
The PL property of the sample has been measured similarly. FIG. 25B shows the
result of PL measurement of InGaAs/GaAs double hetero-junction. A thickness of
InGaAs layer is about 2.5 nm on the (111) A faces. Like FIG. 25A, the abscissa
shows photon energy to emit light in unit of eV while the ordinate shows
strength of PL light emitting in arbitrary unit.

DEPR:
In FIG. 25B, two peaks have been observed in a curve pl2 showing PL strength,
as stated in the double heterojunction structure in FIG. 25A. However, these
two peaks have appeared at energy 1.45 eV and 1.48 eV. It has been found that
the peak at 1.45 eV tends to increase as the layer thickness of **InGaAs** layer is
decreased.

DEPR:
Two PL peaks shown in FIGS. 25A and 25B indicates that the grown **InGaAs** layer
has two kinds of properties.

DEPR:
Such light emitting having different wavelengths can be explained by supposing
that the **InGaAs** layer has respectively different band structures on the top
portion and the side faces.

DEPR:
For instance, it can be considered that In.sub.0.1 Ga.sub.0.9 As has been grown
on the side faces while In.sub.x Ga.sub.1-x As (x>0.1) having larger In
composition has been grown on the top portion. The more In composition in

thickness rc=a.sub.B.multidot.(1+cot(2.alpha.)), a stable point of potential
occurs at the top portion of the pyramid. Where a.sub.B denotes Bohr radius,
and .alpha. denotes hemi-vertical angle.

DEPR:
It may be supposed that the critical thickness is at least 3.multidot.a.sub.B.
In order to exhibit quantum effect fully, it is preferable that the **InGaAs**
layer must be grown to have a thickness of 2a.sub.B or less.

DEPR:
Like this, it can be found that, if an epitaxial layer of a mixed crystal
semiconductor is grown on the side faces of the concave of the triangular
pyramid, the quantum dot can be formed on the top portion of the concave.
Though the shape of the concave is verified experimentally as the tetrahedral
shape, other shapes may attain the same advantages if they have their
sufficiently etching mask, the exposed surface of the substrate 161 is treated
by anisotropic etching using 1 **V** % Br.sub.2 ethanol solution. In the
anisotropic etching, etching rate is extremely lowered on the (111) A faces.
Therefore, the etching ceases automatically when the exposed faces are (111) A
faces.

DEPR:
Then, as shown in FIG. 27G, **InGaAs** quantum well layers 169 of about 5 nm in
thickness, which have their composition In.sub.0.1 Ga.sub.0.9 As on the (111) A
faces, are grown on the surface of the energy barrier layers 168.

higher than that on the (111) B faces.

DEPR:
In other words, the **InGaAs** mixed crystal having high In composition than that of the (111) A faces is grown on the (111) B faces. Therefore, it can be considered that the quantum dots QD are formed by **InGaAs,** which has higher In composition than that of **InGaAs** mixed crystal on the (111) A faces.

DEPR:
FIGS. 28B and 28C show steps of forming electrodes on the surface. An electrode layer 175 may be formed by evaporation etc. on the resultant structure shown in FIG. 27I. The electrode layer 175 is formed by stacking **Ti** lower layer of about 10 nm in thickness and **Au** upper layer of about 200 nm in thickness, for example.

DEPR:
FIG. 28C shows the shape of the electrode from which the resist mask is removed after patterning. The electrodes 175a can contact to the electrode layers 171 by **ohmic contact,** and also exist on the SiO.sub.2 mask 162 around the electrode layers 171.

DEPR:
Furthermore, a layered electrode 190 is formed by stacking **Ti** layer having a thickness of 10 nm and **Au** layer having a thickness of 200 nm on the upper surface of respective layers. The quantum dots QD1 and QD2 are formed on the top portions of the quantum well layers 184 and 186. These quantum dots are

layer and the energy barrier layer repeatedly more over.

DEPR:
Gate electrodes 195 are formed by vacuum evaporation etc. on the side faces of
the mesa type structure. The electrodes 195 are connected to the p.sup.+ type
GaAs layer 192 by **ohmic contact**. The electrode layer 189 formed of n type GaAs
and the n+ type GaAs substrate 161 serve respectively as source and drain. A
gate electrode, to which bias voltage can be supplied, is attached to the
quantum dot QD, which is included between the source and the drain, by the
electrode 195 and the p.sup.+ type GaAs layer 192.

DEPR:
In FIG. 31A, the SiO.sub.2 mask 162 is formed on the surface of the n+ type **InP**
substrate 161. Like the above examples, tetrahedral concaves 164 are formed by
etching. Respective layers are formed by epitaxial growth in the concaves 164
as follows.

DEPR:
First, an n type **InGaAs** layer 196 having a thickness of about 200 nm is grown.
In this case, when **InGaAs** is grown simultaneously on the (111) A faces and the
(111) B faces in the **InP** crystal, mixed crystal composition having higher In
composition are grown on the (111) B faces in contrast to the (111) A faces.
Consequently, line regions having higher In composition are grown in the n type
InGaAs layers 196 on the top of the concaves 164 in the height direction.
Thus, quantum wires QW2 are formed on respective top portions.

199.

DEPR:
Furthermore, In.sub.0.53 Ga.sub.0.47 As layer 197 having a thickness of 200 nm
is grown thereon. In the **InGaAs** layer 197 over the quantum wire QW2, the
quantum wire QW1 as well as the **InGaAS** layer 196 are formed. N type
In.sub.0.53 Ga.sub.0.47 As electrode layers 179a are grown on respective
remaining concave portions.

DEPR:
FIG. 31B shows a structure wherein the pn junction is combined with the
structure of FIG. 31A. The SiO.sub.2 mask 162 is formed on the surface of the
n+ type (or p.sup.+ type) **InP** substrate 161. In FIG. 31B, the procedures of
forming openings in the SiO.sub.2 mask 162 through the tetrahedral concaves 164
are identical to those in FIG. 31A.

DEPR:
In the concave 164, n type **InGaAs** layer 196 of 200 nm in thickness, **InP** layer
198 of 7 nm in thickness, In.sub.0.53 Ga.sub.0.47 As layer 199 of 5 nm in
thickness, **InP** layer 200 of 7 nm in thickness, and In.sub.0.53 Ga.sub.0.47 As
layer 197 of 200 nm in thickness are continuously formed. And, p type
In.sub.0.53 Ga.sub.0.47 As electrode layer 179b is formed to bury remaining
concave areas.

DEPR:
The present invention is not limited by the above descriptions. For example,
the quantum dots and the quanti

 The

epitaxy (MBE) and gas source MBE etc. may be used. The semiconductor materials
used here are not limited to the aboves. For instance, if the quantum well
layer is formed by **InGaAs** on the GaAs substrate, **InGaP** as well as AlGaAs may be
used as the energy barrier layer. In addition, on the **InP** substrate, the
quantum well layer may be formed by **InGaAsP,** and the energy barrier layer may
be formed by InAlGaAsP. Otherwise, it is obvious for the skilled person that
various variations, improvements, combinations and the like are enabled.

DEPR:
In the fourth to sixth embodiments, the SiO.sub.2 mask has been employed to
form the concave section. However, the mask is not restricted to the SiO.sub.2
mask and therefore an insulating film such as a silicon oxynitride film (SiON
film) or a silicon nitride film (Si.sub.3 N.sub.4 film) may be utilized.
Furthermore, a conductive mask such as **W,** WSi, or Al may be used. But, since
it is important that the mask has to be tightly contacted to the substrate to
control the shape of the concave section, the SiO.sub.2 is the most suitable in
view of this respect.

CLPR:
13. The method according to claim 10, wherein said quantum structure comprises
a III-**V** group compound semiconductor layer, and is formed by stacking materials
having large band gap and materials having small band gap in sequence.

elements and a growth temperature.

ORPL:
S. Tsukamoto, et al., Fabrication of GaAs Wires on epitaxially Grown **V** Grooves
by Metal-Organic Chemical-Vapor Deposition, J. Applied Physics, vol. 71, No. 1,
Jan. 1, 1992, pp. 533-535.

ORPL:
D. Leonard, et al., Direct Formation of Quantum-sized Dots, from Uniform
Coherent Islands of **InGaAs** Surfaces, Applied Physics Letters, vol. 63, No. 23,
Dec. 6, 1993, pp. 3203-3205.

ORPL:
J.Y. Marzin, et al., Photoluminescence of Single **InAs** Quantum Dots Obtained by
Self-organized Growth on GaAs, Physical Review Letters, Vo. 73, No. 5, Aug. 1,
1994, pp. 716-719.

ORPL:
H.V. Schreiber, et al., Si/SiGe **Heterojunction Bipolar Transistor** with Base
Doping Highly Exceeding Emitter Doping Concentration, Electronics Letters, vol.
25, No. 3, Feb. 2, 1989, pp. 185-186.

DOCUMENT-IDENTIFIER: US 5804877 A
TITLE: Low-resistance contact on a compound semiconductor

EXA:
Tang; Alice **W.**

EXP:
Whitehead; Carl **W.**

ABPL:
Generally, and in one form of the invention, a method is disclosed for forming an **ohmic contact** on a GaAs surface 20 comprising the steps of depositing a layer of **InGaAs** 22 over the GaAs surface 20, and depositing a layer of **TiW** 24 on the layer of **InGaAs** 22, whereby a reliable and stable electrical contact is established to the GaAs surface 20 and whereby **Ti** does not generally react with the In.

BSPR:
It is well known that low resistance ohmic contacts to GaAs are difficult to obtain due to a 0.8 eV Shottky barrier associated with the metal-GaAs interface. It is also known in the art that the metal-**InGaAs** interface produces a nearly zero Shottky barrier height and hence a low contact resistance. **Ohmic contact** may be made to GaAs by interposing an In.sub.x Ga.sub.1-x As layer, with x=0 at the GaAs interface and graded to x.apprxeq.0.8 at the metal-**InGaAs** interface, between the GaAs layer and the metal contact.

at the device level. Specifically, AuGe/Ni/Au, Ti/Pt/Au, and AuZn are a few of the metallization schemes that have been used to make contact to GaAs as well as to **InGaAs**. However, as demand for better device performance continues to increase, the need for a lower resistance contact scheme to **InGaAs**, in particular, has become apparent.

BSPR:
As has been stated hereinabove, the use of an interposed layer of **InGaAs** to form contact between a metal and GaAs is known in the art. However, the inventors hereof have found that **Au**-based metallization schemes, such as AuGe/Ni/Au, are susceptible to spiking. In efforts to overcome this problem, a refractory metal-based stack, such as Ti/Pt/Au has been used. This metallization, however, has been found to produce a contact that is unstable and generally high in contact resistance, apparently because the **Ti** reacted with the In. Indeed, another **Ti**-based metal, nitrided **TiW**, i.e. **TiW** sputtered in the presence of N.sub.2, was used in the belief that the N.sub.2 would keep the **Ti** from reacting with the In in the **InGaAs**. This, however, suffered from poor adhesion and high compressive stress.

BSPR:
In further experimentation by the inventors, **TiW** was used as a contact on **InGaAs**. Surprisingly, this contact scheme has proven to have a low resistance and is stable. Surprisingly, the **Ti in the TiW** film appears to be sufficiently

of **InGaAs,**
whereby a reliable and stable electrical contact is established. In another
form of the invention, an **ohmic contact** to a GaAs surface is disclosed, the
ohmic contact comprising a layer of **InGaAs** over the GaAs surface, and a layer
of **TiW** on the layer of **InGaAs**. In still another form of the invention a
bipolar transistor is disclosed. The transistor comprises a mesa, and the mesa
comprises a first semiconductor layer, a layer of **InGaAs** atop the first
semiconductor layer; and a layer of **TiW** atop the layer of **InGaAs**.

BSPR:
In addition to its advantage in contact resistance, **TiW** has been proven to
provide superior adhesion as compared to nitrided **TiW** possibly because **TiW**
exhibits less undercutting when etched with common etchants than does nitrided
TiW. Also, as disclosed in **co**-assigned U.S. Pat. No. 5,055,908, **TiW**
possesses the advantage of selectable stress, i.e. the stress of the **TiW** film
(over a broad range from compressive to tensile) is found to be dependent upon
sputter deposition pressure. Nitrided **TiW,** on the other hand, has been found
to produce only a compressively stressed film. The ability to select stress in
metallic films is known to be important in producing reliable contacts between
dissimilar materials under conditions such as temperature cycling.

DEPR:
An advantage of this invention can be the formation of a stable, reliable, and

therefore a
lower contact resistance. The choice of the metal in the contact system has
proven to be another way to lower the contact resistance. Commonly used
metallization schemes such as AuGe/Ni/Au and Ti/Pt/Au produce high resistance
contacts that also suffer from reliability problems. AuGe/Ni/Au is susceptible
to spiking through the **InGaAs,** and when Ti/Pt/Au was used on highly doped
InGaAs by the inventors hereof, the resulting contacts corroded over a short
period and the contact resistance increased by more than a factor of three. It
is believed that the **Ti** reacted with the In to form a highly resistive
intermetallic compound. Consequently, contact systems in which **Ti** was not
present (WSi, for example) were used, but also resulted in a high resistance
contact that suffered from the additional disadvantage of providing a highly
undercut etch profile.

DEPR:
In further experimentation, **TiW** that had been sputtered in the presence of
N.sub.2 was used in the belief that the N would bind the **Ti** to keep it from
reacting with the In. However, this contact suffered from poor adhesion due to
deep undercutting at the metal-**InGaAs** interface. However, in another
experiment, **TiW** was tried on **InGaAs** because it was readily available, although
there was little hope of the **Ti** not reacting with the In. Surprisingly, the
contact as deposited possessed a low resistance whereas other systems required
anneal or alloy conditions to

DEPR:
The TiW/InGaAs contact has been found to promote less undercutting than does nitrided **TiW**. Plasmas containing F seem particularly to etch at the nitrided **TiW-InGaAs** interface more so than at the **TiW-InGaAs** interface. It should be noted that a similar etch difference has been observed with wet chemical etches as well.

DEPR:
Additionally, **TiW** can be induced, through the selection of the proper sputter deposition pressure, to create a layer whose stress varies from about 5.times.10.sup.10 dynes/cm.sup.2 compressive to about 5.times.10.sup.10 dynes/cm.sup.2 tensile. The ability to select the stress that a layer possesses in a finished structure is important in preventing delamination and cracking in temperature-stressed structures comprising layers of dissimilar materials. This particular aspect of **TiW** layers was addressed in **co**-assigned U.S. Pat. No. 5,055,908.

DEPR:
In a preferred embodiment of the invention, shown in FIG. 1, a 1750.+-.750 Angstrom layer of **TiW** 24 (generally 5-20% wt. **Ti** and 80-95% wt. **W** and more preferably about 10% wt. **Ti** and 90% wt. **W**) alloy is sputter-deposited on a layer of **InGaAs** 22, typically In.sub.0.5 Ga.sub.0.5 As, which has been deposited on a GaAs wafer 20. In another embodiment, it is desired to establish a low resistance con

DEPR:
In this embodiment, an emitter-up configuration is described, though one may
appreciate that a collector-up transistor may be similarly fabricated. The
material structure is shown in FIG. 2. The transistor is fabricated on a
semi-insulating GaAs substrate or wafer 26, for example, and comprises: a
subcollector layer 28, typically GaAs approximately 1.0 .mu.m in thickness and
doped with Si for example to a concentration of approximately
1.5.times.10.sup.18 cm.sup.-3 ; a collector layer 30, typically GaAs,
approximately 0.65 .mu.m in thickness and doped with Si for example to a
concentration of approximately 8.0.times.10.sup.15 cm.sup.-3 ; a base layer 32,
typically GaAs, approximately 0.05 .mu.m in thickness and doped with C for
example to a concentration of approximately 1.5.times.10.sup.19 cm.sup.-3 ; an
emitter layer 34, in this embodiment of AlGaAs but may alternatively be of
GaInP, approximately 0.1 .mu.m in thickness and doped with Si for example to a
concentration of approximately 5.times.10.sup.17 cm.sup.-3 ; a buffer layer 36,
typically GaAs, approximately 0.15 .mu.m in thickness and doped with Si for
example to a concentration of approximately 3.times.10.sup.18 cm.sup.-3 ; and
an **InGaAs** cap layer 38 approximately 0.05 .mu.m in thickness and doped with Si
for example to a concentration of approximately 1.times.10.sup.19 cm.sup.-3.
As in the first embodiment, a **TiW** layer 40 is sputtered on the **InGaAs** layer 38,
as shown in FIG. 3.

about 90.degree. C. for approximately 90 seconds. The wafer is then blanket
exposed at 365 nm for about 0.7 seconds, track baked at about 125.degree. C.
for approximately 50 seconds, exposed in a stepper apparatus, and batch
developed in a solution of 1:1, photoresist developer and water, for about 6
minutes. The exact conditions will vary with resist batch, as will the bakes,
blanket exposure, pattern exposure, and develop times for optimum resist
sidewall profile also change. This process leaves the **TiW** surface exposed in
the desired location of the emitter contact, as shown in FIG. 4.

DEPR:
Following the formation of the image reversal photoresist pattern, the wafer is
submitted to a descum or light ash to remove resist or other organic residues
in the pattern, dipped in buffered HF (Bell #2 for example) to remove surface
oxides, rinsed and spin rinse dried. **Au**-based emitter metallization 44 is
evaporated onto the wafer, depositing through the openings in the photoresist
onto the previously deposited **TiW** contact layer, as shown in FIG. 5. The
photoresist is then "lifted-off" by attacking it with a solvent at patterned
region sidewalls not covered by the evaporated metal. Because the wafer
surface is entirely covered with metal (**TiW**) prior to the evaporation, the
radiant energy from the metal evaporation source will be more efficiently
collected than when the wafer is bare GaAs. This can result in excessive
heating of the photoresist, thereby altering the profile such that evaporated

(400 Angstroms)/ **Au** (3800 Angstroms), for example. In order to ensure minimum heating during this evaporation, the **Ti** rise, soak, and predeposition times are set at about 5 seconds each. This permits the **Ti** to be ready to evaporate when the system shutter opens without spending excessive time at each of these processes, thereby resulting in much less damage to the resist profile from radiant heating during evaporation of the **Ti**. For similar reasons, **Pt** rise, soak and predeposition times are set at about 5, 5 and 15 seconds, respectively.

DEPR:
Following evaporation, the photoresist is lifted off in solvent, leaving the structure shown in FIG. 6. Typically, acetone is employed with soaks, ultrasonic agitation or spraying while the wafer is being spun. While the details of the lift-off process can adversely affect the patterning results, almost any process that leaves a debris-free surface is suitable. The resulting patterned metal 44 is used as a mask to etch the emitter geometry into the **TiW** and then into the semiconductor underneath.

DEPR:
An alternative method of forming the emitter geometry involves sputtering sequential layers of **TiW then Au** over the wafer, spinning photoresist, exposing and developing the pattern, and then pattern etching the **Au and TiW** layers to form the emitter metal geometry which serves as a pattern mask for wet chemical or reactive ion etching of the

metal is put
down in a single vacuum deposition.

DEPR:
In order to form the emitter mesa of the transistor, a selective reactive ion
etching (RIE) process is employed to etch through the **TiW** 40, stopping on the
InGaAs 38 surface. The resulting structure is shown in FIG. 7. The **InGaAs** 38
is etched in a non selective, timed, wet etch which results in the structure of
FIG. 8. The GaAs buffer 36 is etched in a Reactive Ion Etch process that stops
on the AlGaAs emitter layer 34, giving a positive reference for etching the
balance of the emitter region in a controlled rate, controlled undercutting,
timed RIE etch permitting precise control for stopping safely in the 500 to
1000 angstrom thick p+ GaAs base region 32. For example, the **InGaAs** layer 38
is wet etched for a sufficient time to clear and etch into the GaAs buffer 36.
The GaAs is RIE etched in a gas mixture that will not etch AlGaAs, and thus the
etch stops on the AlGaAs emitter layer 34. The distance to the thin p+ base
region 32 is precisely known at this point. Without the selectivity of the
initial RIE etch with respect to AlGaAs, costly and inaccurate step height
measurements would be required after the **InGaAs** wet and GaAs RIE etch to ensure
etching into but not through the base region 32. An illustration of the
structure, etched to the top of the AlGaAs layer, is shown in FIG. 9. It may
be appreciated that a similar selective etch procedure could be applied to
emitter layers comprising mate

debris, and the surface of the unetched **TiW** 40 is generally free of any
possible etch masking contaminant. The final plasma ash, which may be
performed in either a radio frequency plasma reactor or in a microwave
frequency down stream reactor in O.sup.2, O.sub.2 :He, or O.sub.2 :N.sub.2 O,
or similar gas mixtures, is an important last step prior to RIE etching of the
TiW contact 40.

DEPR:
The wafers are immediately placed in an RIE apparatus. The **TiW** 40 is etched in
CF.sub.4 +8% O.sub.2 @ 250 watts, 30 millitorr, 40.degree. C., for example, to
a visible clearing of the **TiW** layer 40 plus 50% over-etch. The etch stops on
the **InGaAs** 38 and undercuts the **TiW** layer by about 1500 angstroms or less.
Following RIE of the **TiW** 40, the wafers are lightly cleaned through a water
spin-rinse dry. The **InGaAs** layer 38 is then removed in a 1:8:160 solution of
H.sub.2 SO.sub.4 :H.sub.2 O.sub.2 :H.sub.2 O for about 25 seconds. The
solution is mixed fresh, and allowed to age for about 30 minutes prior to using
to establish a repeatable etch rate for the process. The wafers are rinsed in
flowing deionized water, then spin-rinsed and dried.

DEPR:
In order to ensure removal of any masking organic residue, the wafers are ashed
for about 5 minutes at 150 watts, 900 millitorr in a barrel type asher, etched
30 seconds in 40:1 NH.sub.4 OH, rinsed in flowing deionized water, then
spin-rinsed and dried prior to

angstroms/minute, and is timed to etch to the AlGaAs emitter layer 34 with about 50% over etch. The timing is not critical since the etch does not appreciably attack the AlGaAs emitter layer 34. Further, since the etch depth is to the graded AlGaAs emitter layer 34 surface, the remaining etch depth to the approximately 1000 Angstrom thick p+ base region 32 is precisely known from the original HBT epitaxial structure. As a check on the process and to serve as a reference for the next and more critical etch to base step, etch step heights are measured at 5 positions on the wafers. This step height results from the composite thickness of the **TiW** 40, **InGaAs** 38, and GaAs 36 layers above the AlGaAs emitter 34. In another preferred embodiment of this process step, BCl.sub.3 +SF.sub.6 may be substituted for CCl.sub.4. The SF.sub.6 keeps BCl.sub.3 from etching AlGaAs, which it would otherwise. Surprisingly, it appears that a variety of etchants fulfill the requirements of etching GaAs, but stopping on AlGaAs. CCl.sub.4 is just one gas in the group that includes Chlorocarbons and Chlorofluorocarbons that, when used in a RIE arrangement, etches GaAs, but stops on AlGaAs. Additionally, it appears that non-Ar Cl-based gases in general, of which BCl.sub.3 is one, when used with a source of F, like SF.sub.6, will also perform the required etch (Ar appears to increase the sputter rate and can make the etch less likely to stop on AlGaAs, He appears to have benefits over Ar as a buffering gas). The non-C-containing etches also

base region 32. However, Cl will remain from the etch and can cause corrosion
of the **Au** contact 44 under bias conditions. This Cl can be removed by exposure
to rf plasma in CF.sub.4. Pilot wafers are etched to verify and recalibrate
etch rate in the reactor prior to etching the device wafers. In a preferred
embodiment of this invention, the etch to base process is performed as follows:

DEPR:
b. Wafers are loaded into the RIE chamber. Gas flows (BCl.sub.3 @ 200 sccm, 4%
H.sub.2 in He @ 30 sccm, and Cl.sub.2 @ 8 sccm) are established at 50
millitorr. Wafers are RIE etched, by time established in etch rate
determination and etch distance, to base 32 in those gases at a dc bias of -45
v. A probe for surface breakdown is employed for verification of etch to base
32.

DEPR:
The total etch process (through the **TiW** 40 to the p+ base 32) results in
undercutting the emitter contact pattern such that overhang of the **TiW-Ti-Pt-Au**
emitter geometry pattern shadows the emitter mesa side walls, as shown in FIG.
10, thereby permitting self aligned base contacts with normal incidence
evaporation. If non-self-aligned base contacts are used, the emitter mesa
undercut ensures that close placement misalignment does not result in
emitter-base shorting.

DEPR:
In a preferred embodiment of telf-

differ. **Ti-Pt-Au** films, in thicknesses of 500, 250, and 1500 Angstroms 48 are sequentially evaporated and lifted off. Film thicknesses are deliberately low to ensure that with close to emitter placement, or with self alignment, the top of the base contact will be safely below the emitter metal. Post lift-off clean-ups are essentially the same as with the emitter **Ti-Pt-Au** process. The structure, with base contacts, is shown in FIG. 11.

DEPR:
In a specific embodiment of this invention, the wafers are etched 30 seconds in 40:1 H.sub.2 O:NH.sub.4 OH, rinsed in flowing deionized water, and spin rinse dried. Adhesion promoter is applied, and positive photoresist is spun on, baked, aligned, exposed, developed, ashed 3 minutes at 150 watts, 900 millitorr in a barrel type asher, and baked 30 minutes @ 100.degree. C. The wafers are again ashed 3 minutes at 150 watts, 900 mt in a barrel type asher. At this point, the resist thickness is measured to serve as a rough base line for determining etch depth. The wafers are then dipped 10 seconds in buffered HF to remove native oxides, rinsed in flowing deionized water, and spin rinse dried. The wafers are then etched as with the AlGaAs portion of the emitter etch. Time is set from etch rate determination to remove approximately 7700 angstroms. Proper etch depth is verified both with a step height measurement and a probe for surface breakdown. Wafers are then ashed 1 minute at 150 watts, 900 mt in a barrel type asher, etch cleaned 10 seconds in 1:8:160

prevent metal
continuity over resist sidewalls to collector contacts, thus permitting resist
liftoff patterning of the collector contact. Resist and excess metal are
removed by solvent liftoff, and ashed 5 minutes at 150 watts, 900 millitorr in
a barrel type asher to remove organic residues. The resulting structure is
shown in FIG. 14.

DEPR:
a. Following the ash step above, wafers are plasma pre-treated at 15 **W,**
50.degree. C., and 260 millitorr in a gas mixture of Freon 13B1 and CF.sub.4
+8% O.sub.2 to enhance Si.sub.3 N.sub.4 adhesion and reduce plasma induced
damage from nitride and oxide deposition.

DEPR:
For example, an embodiment of the invention has been described hereinabove.
This embodiment was an HBT of the emitter-up type, i.e. contact was made to an
emitter mesa that protrudes from the surrounding substrate. As may be
appreciated, the invention described herein may also be applied to HBTs of the
collector-up type, an example of which is shown in FIG. 15. This transistor is
similar to the emitter-up type in that it comprises a stack of selectively
etched semiconductor layers on a semiconductor substrate 49. On the substrate
49 is placed an emitter contact layer 50 of n+ GaAs for example; an emitter
layer 52 of n-doped AlGaAs or of GaInP for example; a base layer 54 of p+ GaAs,
a buffer layer 56 of GaAs or AlGaAs for example, a collector layer 58 of GaAs

etch rate
differential for plasma etchable interconnects or resistors, and
good faceting
for planarization sloping by ion milling or sputter etching.

CLPR:
1. An **ohmic contact** to a GaAs surface comprising:

CLPR:
2. The **ohmic contact** of claim 1 wherein said layer of **InGaAs** is
In.sub.0.5
Ga.sub.0.5 As.

CLPR:
3. The **ohmic contact** of claim 1 wherein said layer of **InGaAs** is
doped with Si
to a concentration of approximately 1.times.10.sup.19 cm.sup.-3.

CLPR:
4. The **ohmic contact** of claim 1 further comprising a composition
of metal on
said layer of **TiW,** said composition of metal containing **Au**.

CLPR:
5. The **ohmic contact** of claim 4 wherein said composition of
metal comprises
Ti, Pt, and Au.

CLPR:
8. The transistor of claim 6 further comprising a composition of
metal on said
layer of **TiW,** said composition of metal containing **Au**.

CLPR:
9. The transistor of claim 6 wherein said layer of **InGaAs** is
In.sub.0.5
Ga.sub.0.5 As.

CLPR:
11. The bipolar transistor of claim 10 wherein said emitter mesa
further

CLPW:
a layer of **InGaAs** atop said first semiconductor layer; and

CLPW:
a layer of **TiW** ohmically contacting said layer of **InGaAs**.